Recent Developments in Vertical Bloch Line Data Storage

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Abstract

Data storage systems based on vertical Bloch lines have been fabricated in 2 μm bubble garnet material. The input/output line was fully operational, and experiments in reading and writing showed an encouraging correlation between input and output. Further effort is required to solidify these processes and to establish bit propagation around the storage domains.

Introduction

Magnetic data storage systems usually use one magnetic domain to store each bit, but in 1983 Konishi [1] showed that entire data strings could be stored in the wall of a domain. Putting a "twist" (or vertical Bloch line) in a section of wall could encode a "1", while leaving the section untwisted would store a "0". The resulting system would be nearly ideal, storing $\geq$ 1Gb/cm^3 in a modular, radiation hard, rewritable solid state device.

In addition to the storage region, which contains long "stripe" domains whose walls will store the information, a practical vertical Bloch line (VBL) data storage chip requires an input/output line, and write/read gates. In the input/output (I/O) lines electronic data are converted to the presence or absence of magnetic "bubble" domains and vice versa. For writing, these domains are moved into the read/write gates to prevent the creation of VBLs in selected stripes. For reading, the presence of a VBL in a stripe is converted to the presence of a bubble in the write/read gate. The pattern of VBLs can be shifted around the storage stripe by bias field pulses. The storage system is completed with a permanent biasing magnet, small pulse coil, and control electronics.

Domains, Walls, and Bloch Lines

The thin film garnet materials used in bubble memories and vertical Bloch line memories are characterized by strong anisotropy favoring orientation of the spins along the film normal. This energy competes with the usual exchange interaction, which minimizes the deviation between neighboring spins, the demagnetization energy, and the energy of applied fields resulting in domain and wall configurations.

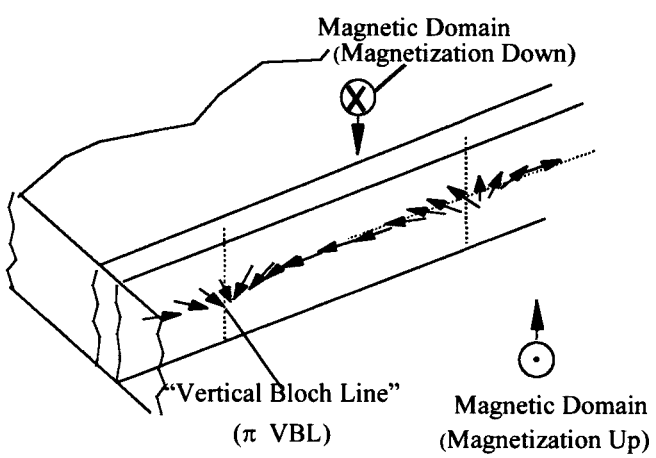

Figure 1. Representation of domains separated by a Bloch wall containing two vertical Bloch lines.

The structure of the domain wall varies through the thickness of the film, but we will focus on only the spins at the center of the film, as are drawn in Figure 1. Reference 2 provides more detail on domain wall structure and vertical Bloch line memory. In passing through the wall from "up" to "down," the magnetization rotates in a plane perpendicular to the plane of the film, characteristic of a Bloch wall. The rotation can be either clockwise or counter clockwise, and both senses of rotation can be sustained in the same wall. However, where two regions of opposite orientation meet, the transition must be a gradual rotation of the magnetization in the plane of the film. These transition regions are called "vertical Bloch lines." The sense of this rotation ("chirality") can also be either clockwise or counterclockwise. If a counterclockwise (-) and a clockwise (+) VBL meet, they will unwind, but two VBLs of the same chirality can form a stable bound pair, or a 2π VBL.

VBLs are formed when walls move at a critical velocity. A region of "opposite" chirality nucleates at one surface and grows through the thickness of the material as the wall advances. If the reversed region grows all the way through the film, a vertical Bloch line will have been formed on either side of it, one + π and one -π. If the wall continues to be driven so hard, another reversed region will start and additional pairs of VBLs may form. Thus, one critical concern for VBL data storage is controlling domain expansion so that only one pair is formed. A second concern arises from the fact that this process creates a VBL of each sign, which will annihilate each other when the wall retreats. Thus, one of them must be removed before the domain relaxes to its previous position.

Single VBLs can move in response to an in-plane field parallel to the domain wall, as can be seen by considering Figure 1. They also move gyrotropically when the wall moves. Positive and negative VBLs move to the left and to the right, respectively, relative to the direction of the wall's motion.

Architecture and Operation

A VBL data storage chip is shown conceptually in Figure 2. In the center lies the storage region. It contains a set of relatively deep partial grooves for stabilization of stripe domains intersected by lesser grooves, which define bit positions [3], and a conductor to nucleate the stripes.

At either end of each stripe-stabilization groove lies a write/read (W/R) gate. These are partially grooved and overlaid with several conductors: the stripe expander, the stripe chopping conductor, and several straight, broad conductors for creating in-plane fields and moving bubble domains between the W/R gate and the Input/Output line. The I/O line consists of a channel (partial groove or ridge) that stabilizes and guides the bubbles, and two serpentine conductors, which create gradients to move the bubbles. At

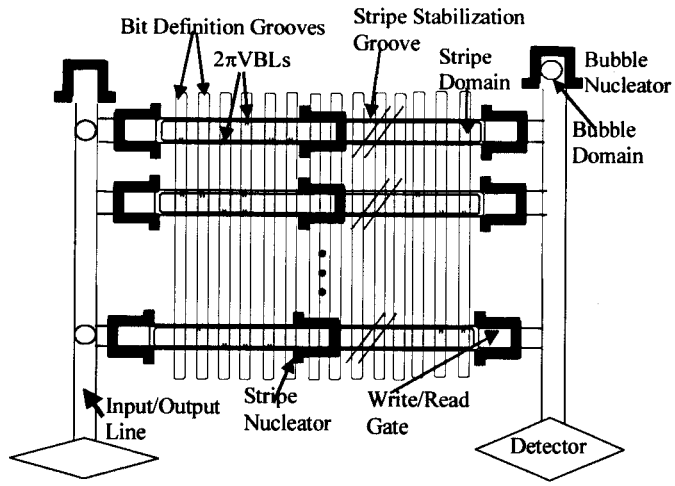

Figure 2 Conceptual layout of a VBL data storage chip. In the center lies the storage area, accessed from either end by write/read gates and input/output lines.

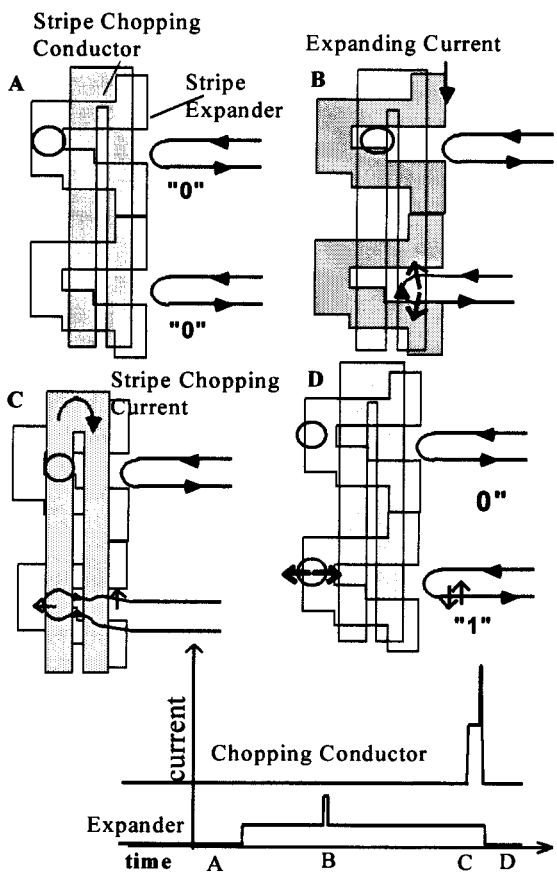

Figure 3. Write Process: A- Bubble pattern has been transferred into the write/read gates to store a "0" in the upper stripe and a "1" in the lower. B- Expansion and creation of a clockwise and counterclockwise VBL in the lower stripe head. C- Sideways motion separates the 2 VBLs. D- A bubble is chopped off the lower stripe and additional VBLs are created. Inset are typical waveforms for the two conductors.

one end of the I/O line lies a bubble nucleator and at the other is a "bubble detector." The detector is a magnetoresistive element, which responds to the stray fields from an elongated bubble. A differential detection scheme is used, with the signal from the "active detector" subtracted from that of a "dummy" detector which is placed further down the I/O line. The "dummy" never encounters a bubble because an "annihilator," a ring-shaped conductor which locally raises the bias field so that the bubble will collapse, is placed between the two detectors. Reliable annihilation was one of the program's recent successes.

Figure 3 depicts the write process using the "notched expander" [4]. In A, a bubble has been placed in the write/read gate to prevent creation of a 2πVBL in the upper stripe. With the bubble pattern in place, the stripe expander is fired (B). The lower stripehead moves so quickly that a $+\pi$ and a $-\pi$ VBL are formed. The sideways motion of the head as it continues into the expander forces the $+\pi$ VBL to the tip of the stripe and the $-\pi$VBL further down the flank. In C, the chopping conductor is pulsed, raising the bias field beneath it and pinching off the tip of the stripe. In the process, another $-\pi$ VBL is formed in the stripe to create a -2π VBL. Magnetostatic repulsion between the bubble and the stripe head has prevented the upper stripe from expanding and chopping; so it doesn't acquire a -2π VBL (D). Typical waveforms for the expander and chopping conductor currents are shown in the inset to Figure 3. The "spike" near the beginning of the expansion pulse accelerates the stripehead briefly so exactly one pair of VBLs is formed before the stripehead moves sideways. The chopping pulse is designed to bring the walls together gently, without changing their VBL structure, and then nip the bubble off cleanly cf. [5] and [6].

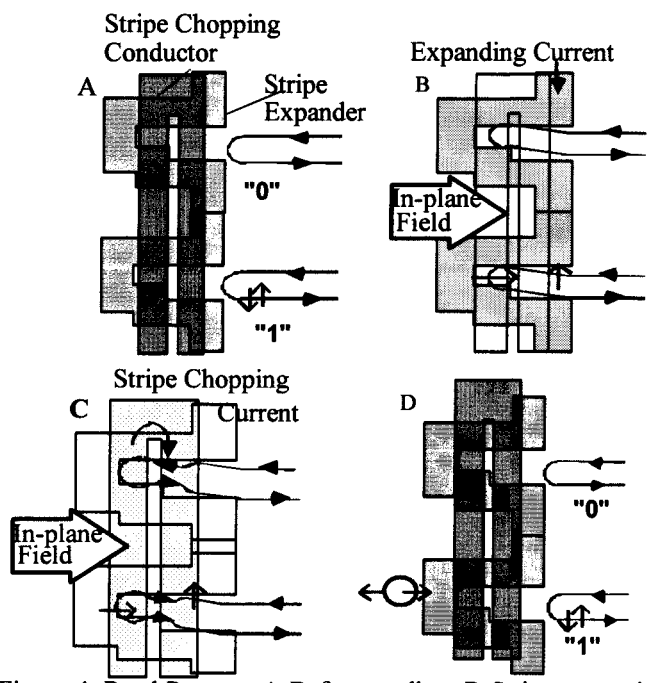

Figure 4. Read Process: A-Before reading. B-Stripe expansion with in-plane field to separate 2π VBL. C-chopping. Note that the spins in the wall beneath the chopping conductors are parallel for the "1" and antiparallel for the "0." D- "1" is represented by a bubble in the I/O line, and the data is ready to be sent to the detector.

Readback is shown in Figure 4. In A, the data of interest has been brought into position near the write/read gate, ready to be read. All the stripes are expanded into the gate (B). An in-plane field is applied to split the 2πVBL into two π VBLs, one on either side of the chopping conductor. Thus, in the lower stripe the spins in the walls lying beneath the chopping conductor are parallel to each other, while in the stripehead without VBLs they are antiparallel, as shown in C. Due to the exchange interaction, it is easier to bring together parallel than antiparallel walls. So, with an appropriate choice of chopping conductor current only the lower stripe will be broken into a stripe and a bubble. In D the bubble pattern is ready to be moved down the I/O line to the bubble detector. Typical waveforms for the read process are similar to those for write. Only the lower current is used in the expander, though, and the height of the chopping pulse spike is the same or lower.

Experiments and Results

The recent vertical Bloch line data storage activity at JPL used yttrium iron garnet material that supported 2 μm wide stripe domains, purchased from Litton and from Shin-Etsu. Their characteristics are summarized in Table 1. The greater contrast between domains in the Litton material made it convenient for microscopic observation.

These chips were fabricated by the Honeywell Technology Center.

The VBL memory test bed consisted of an optical system to image the domains using the Faraday effect, a set of Hewlett Packard 8110 and 8114 pulse generators to provide currents to the on-chip conductors, and air core electromagnets to provide uniform normal and in-plane fields across the chip, and a computer. Chip operation can be monitored electronically using the detectors themselves, but most of our work relied on optical observation of the domains.

Early efforts at JPL focussed on good operation of the I/O line [7]. A reliable, fast major line is key to the speed performance of VBL data storage and enables electrical, as opposed to optical, data acquisition during further development of the chip. In 1996, 2 MHz operation was demonstrated. Since then the I/O lines have regularly run at 1 MHz and 100kHz. The pulse sequence consists of quarter-period square waves (rise and fall times nominally 2ns), with coincident edges. The same currents, ±35 mA in Metal 2 and ±45 mA in the Metal 3 conductor, work well for both Litton and Shin-Etsu material. Another early goal that has been achieved was functionality of all parts of the device at the same bias field.

More recently we concentrated on writing and reading VBLs using the notched expander. The first step was to identify sets of expansion and chopping pulses for writing and reading by measuring the threshold current for chopping as a function of the expander current "spike" height. These values varied from chip to chip and from stripe to stripe on the same chip. Rather than optimize one stripe, we strove to find a group of stripes on the same chip that operated reasonably with one set of conditions. This provided a more uniform basis for comparison and sped up data acquisition. The chips contained variations in spacing between stripes, in the orientation of the stripe nucleator relative to the orientation of the expanders,

Parameter	Description	Litton	Shin-Etsu
h (μm)	Thickness	2.43 ± 0.05	1.78 ± 0.04
$4\pi M_s$ (G)	Saturation magnetic flux density	476 ± 3	372 ± 3
H_K (10^3 Oe)	Anisotropy field	1.60 ± 0.03	2.31 ± 0.08
H_{co} (Oe)	Collapse field	251 ± 1	151 ± 3
α	Gilbert damping parameter	0.11	0.12

Table 1. Characteristics of the garnet materials used.

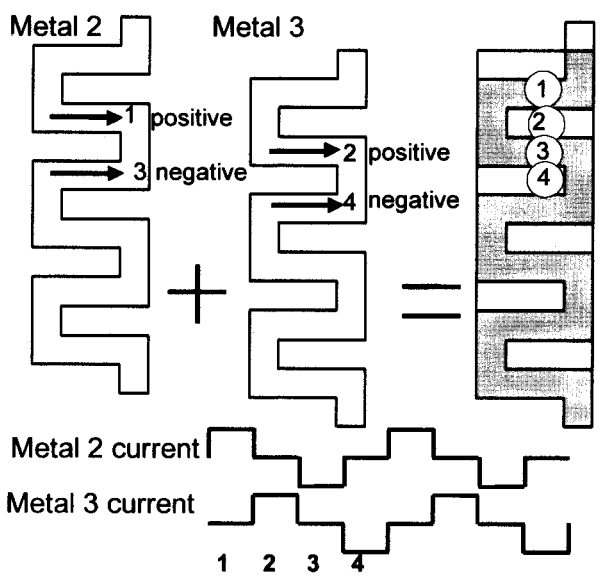

Figure 5. Representation of the I/O line. At upper left are the Metal 2 and Metal 3 serpentines and their current at different points in the cycle. At upper right is their superposition and the positions of the potential minimum for the bubble at each part of the cycle and at bottom are the waveforms.

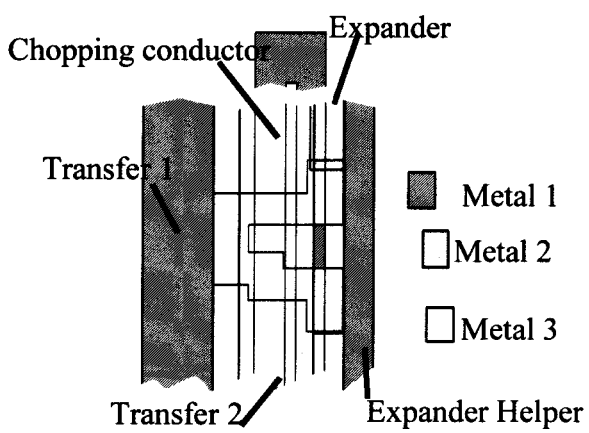

Figure 6. Detailed view of the W/R gate used in these experiments. Only the metallization, not the grooving, is shown. Metal 1 is closest to the garnet.

and in bit definition grooving. Two chips from neighboring die on the same Litton wafer were chosen for further study. The stripes selected were spaced 32 μm apart, had no bit definition grooves, and were created by nucleators which "opened" the opposite direction as the expanders.

With their sets of pulse parameters in hand, we attempted partially operating the chips: writing and reading in succession. New storage stripes were created every trial. No attempt was made to clear the stripes of existing VBLs.

Writing proceeded approximately as described above, and stroboscopic microscopy confirmed that the domains moved in the write/read gates as expected. Practice deviated from the scheme of Figure 3, however, in one respect. After the bubbles were transferred into the write/read gates, a small (50 mA) current was sent through the "expander helper" conductor to move the stripeheads further back in their stabilization grooves because it improved performance. No good alternative was found by decreasing the transfer conductor(s)' currents in the time available. This interaction between the transfer conductors and the stripes requires further investigation.

After writing, at point D in Figure 3, the bubbles had to be removed from the gates. In practice, they would probably be transferred into the I/O line and propagated through the detector to the annihilator. In our limited experiments, readback was less successful if the bubbles were transferred from the gates and propagated away, than if they were annihilated in the gates by pulsing large currents (+and – 150 mA) through the Transfer1 and Transfer 2 conductors. This simply indicates further interaction between the transfer conductors and the stripeheads. Helmholz coils were energized to create a ~8 Oe in-plane field. (Ultimately, on-chip conductors should provide this in-plane field. Also, the small size of the field raises questions for further investigation.) All the stripes were then expanded and subjected to a chopping pulse. The resultant bubbles, if any, were noted. The experiment was repeated with a variety of data patterns. Figure 7 presents data from these investigations.

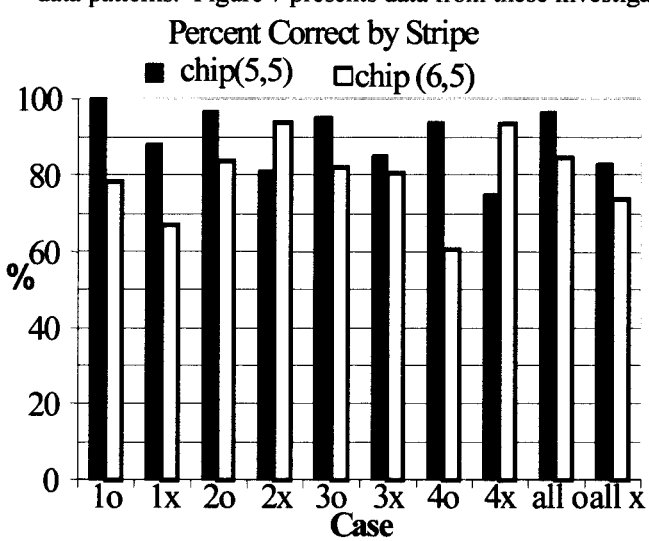

Figure 7. Those responses which were "correct" as a percent of all trials, by stripe. "X" indicates that the stripe was blocked during writing, and "O" indicates that the stripe was not blocked.

"Percent Correct" means the fraction which chopped on readback if they had not been blocked during writing which did not chop on readback if they had been blocked during writing. 170 trials were made on chip (5,5), 365 on chip (6,5).

In another set of experiments the read process was repeated a second time as soon as the stripes had returned to their grooves, without any attempt to move VBLs. A thorough investigation of this kind could provide insight into the way π VBLs move, how VBLs bind, and the effects of the read process. After the first read, the stripes returned to the stabilization grooves, the results were recorded, and any bubbles eliminated. The in-plane field was not removed. The expansion and chopping pulses were repeated, and the resulting bubble pattern recorded. 53 trials were made on chip (5,5), 186 on chip (6,5). The same type of data as Figure 7 for just the first of the two reads is shown in Figure 8. The fact that they differ so much might be an artifact of the small sample size. Figure 9 presents those trials in which the stripe did the same thing (either "right" or "wrong") both times it was read, as a percentage of all the trials. The high rate of repeated results indicates, perhaps, that this read process does not change the state of the stripe.

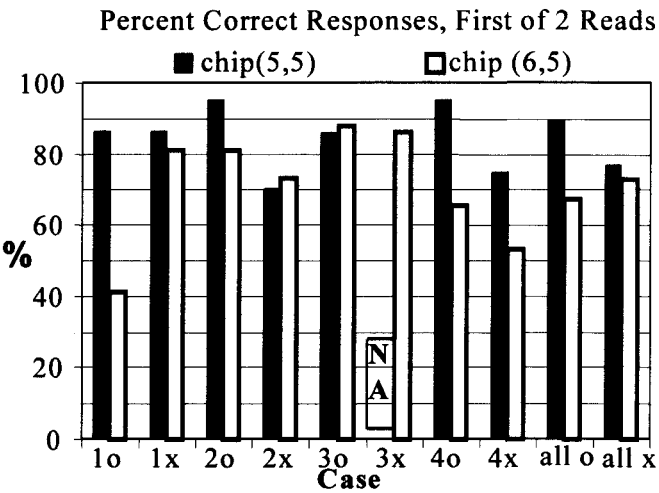

Figure 8.Like Figure 7, but for the first of the two reads.

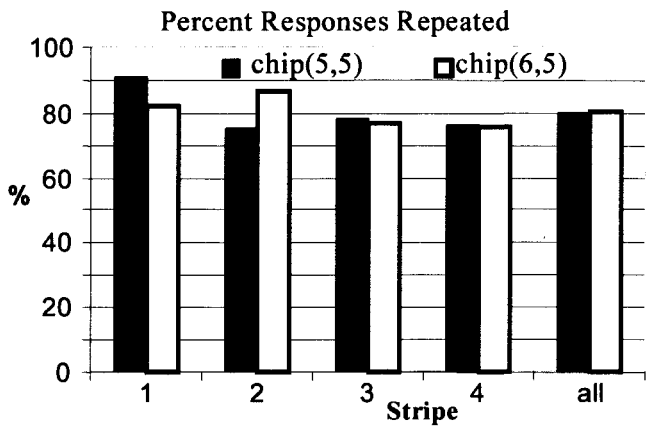

Figure 9. Of the trials, those in which the stripe did the same thing, either "right" or "wrong," on both reads.

Conclusions

Vertical Bloch Line data storage technology presents much promise, although its development has been slow and difficult. However, many of the foundations for a successful storage system have been laid, namely: I/O lines and write/read gates that operate at the same bias field, functional electronic detection schemes, fast I/O lines, and perhaps even operational write/read gates.

Acknowledgements

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Date: 12/4/97

INNOVATOR REPORT

Romney R Katti

NTR No.	Item No.	NTR Title	Tech Brief Title	NMO Ret.	CIT Ret.	Publication Date
NPO-17954	7452	HIGH SPEED MAGNETO-RESISTIVE RANDOM ACCESS MEMORY	FAST MAGNETORESISTIVE RANDOM-ACCESS MEMORY	Yes	No	April 91
NPO-17998	7497	INTEGRATED, NONVOLATILE, HIGH SPEED ANALOG RANDOM ACCESS MEMORY	MAGNETIC ANALOG RANDOM-ACCESS MEMORY	Yes	No	November 91
→ NPO-17999	7499	HIGH SPEED, NON-VOLATILE RANDOM ACCESS MEMORY WITH MAGNETIC STORAGE AND HALL EFFECT SENSOR	MAGNET/HALL-EFFECT RANDOM-ACCESS MEMORY		Yes	November 91
NPO-18010	7503	PHOTOCHROMIC RECORDING PROCESS, SYSTEM AND MEDIA	PHOTOCHROMIC RECORDING PROCESS, SYSTEM AND MEDIA	Yes	No	
NPO-18218	7733	COMPACT MEMORY USING HYBRID MAGNETIC RECORDING TECHNOLOGY	COMPACT TRANSLATING-HEAD MAGNETIC MEMORIES	No	No	May 92
NPO-18219	7735	THICKNESS AND ROUGHNESS DEPENDENCE OF DE MODULATION NOISE IN THIN FILM MAGNETIC RECORDING DISK MEDIA	STUDY OF DC MODULATION NOISE IN MAGNETIC RECORDING DISKS	No		June 92
→ NPO-18467	8000	INTEGRATED VERTICAL BLOCH LINE MEMORY	VERTICAL-BLOCH-LINE MEMORY	No	No	June 93

Date: 12/4/97

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NTR No.	Item No.	NTR Title	Tech Brief Title	NMO Ret.	CIT Ret.	Publication Date
NPO-18529	8069	NONVOLATILE GALLIUM ARSENIDE RANDOM ACCESS MEMORY	NONVOLATILE GaAs RANDOM-ACCESS MEMORY		Yes	March 94
NPO-18533	8074	THREE-DIMENSIONAL MEGNETIC BUBBLE MEMORY SYSTEM	THREE-DIMENSIONAL MAGNETIC-BUBBLE MEMORY SYSTEM		Yes	December 93
→ NPO-18615	8169	NEW READ GATE DESIGN FOR VERTICAL BLOCH LINE MEMORY	IMPROVED READING GATE FOR VERTICAL-BLOCH-LINE MEMORY		Yes	September 94
→ NPO-18626	8173	NEW MEMORY CELL WRITE DESIGN FOR THE MICROMAGNET HALL EFFECT RANDOM ACCESS MEMORY (MHRAM)	IMPROVED WRITING-CONDUCTOR DESIGNS FOR MAGNETIC MEMORY		Yes	June 94
NPO-18627	8174	NEW MEMORY CELL READ-OUT DESIGN FOR THE MICROMAGNET-HALL EFFECT RANDOM ACCESS MEMORY (MHRAM)	IMPROVED READOUT FOR MICROMAGNET/HALL-EFFECT MEMORIES		Yes	September 93
NPO-18628	8175	NEW HALL SENSOR FOR THE MICROMAGNET-HALL EFFECT RANDOM ACCESS MEMORY (MHRAM)	IMPROVED HALL-EFFECT SENSORS FOR MAGNETIC MEMORIES		Yes	September 93

Date: 12/4/97

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	NTR No.	Item No.	NTR Title	Tech Brief Title	NMO Ret.	CIT Ret.	Publication Date
—>	NPO-18644	8196	HALF-STATE READBACK IN VERTICAL BLOCH LINE MEMORY	HALF-STATE READOUT IN VERTICAL-BLOCH-LINE MEMORY		Yes	February 94
	NPO-18726	8285	DOMAIN IMAGING IN MAGNETIC GARNETS USING TUNNELING-STABILIZED MAGNETIC FORCE MICROSCOPY	IMAGING DOMAINS IN MAGNETIC GARNETS BY USE OF TSMFM	No	Yes	September 94
	NPO-18749	8313	PARTIAL GROOVING IN VERTICAL BLOCH LINE MEMORY	PARTIAL-THICKNESS GROOVES IN A VBL MEMORY DEVICE	No	Yes	May 94
	NPO-18750	8314	NEW READ GATE DESIGN FOR VERTICAL BLOCH LINE MEMORY				
—>	NPO-18867	8442	THREE DIMENSIONAL VERTICAL BLOCH LINE MEMORY SYSTEM	THREE-DIMENSIONAL VERTICAL-BLOCH-LINE MEMORY SYSTEM		Yes	July 94
	NPO-19036	8618	NEW DISK CODING SCHEME FOR HIGH DENSITY DISK DRIVES	CODING FOR INCREASED DENSITY OF BINARY DATA STORED ON DISKS	No	No	January 96
	NPO-19092	8619	INTEGRATED THIN FILM POWER CORE	THIN-FILM POWER TRANSFORMERS	No	No	October 95
	NPO-19342	8928	GARNET-OXIDE RANDOM ACCESS MEMORY (GO-RAM)	GARNET RANDOM-ACCESS MEMORY	No	No	November 95

Date: 12/4/97

INNOVATOR REPORT

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NTR No.	Item No.	NTR Title	Tech Brief Title	NMO Ret.	CIT Ret.	Publication Date
→ NPO-20131	9767	JPL'S MAGNETIC RANDOM ACCESS MEMORY: MAGRAM				